FSC-BT909C

5.2 Dual Mode Bluetooth Module Data Sheet

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Release Record

Version Number	Release Date	Comments
Revision 1.0	2022-07-8	First Release
Revision 1.1	2022-07-11	Add application principle diagram
Revision 1.2	2022-07-11	Restricted Area Size correction
Revision 1.3	2022-08-29	Pin description changed
Revision 1.4	2022-11-28	Update Bluetooth version to 5.2

1. INTRODUCTION

FSC-BT909C is a bluetooth 5.2 Smart Ready device (with BR/EDR & LE support simultaneo usly) . It is a small form factor, highly power and highly economic Bluetooth radio module that allows OEM to add wireless capability to their products. The module supports multiple interfaces that make it simple to integrate into fully certified embedded Bluetooth solutions.

With AT programming interfaces, designers can easily customize their applications to support different Bluetooth profiles, such HS/HF, A2DP, AVRCP, OPP, DUN, SPP, and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) and delivers up to 3 Mbps data rate for distances to 100M.

The module is an appropriate product for designers who want to add wireless capability to their products. The supported remote devices' OS are iOS, Android, and Windows.

External whip antenna, transmitting over 2000M.

1.1 Block Diagram

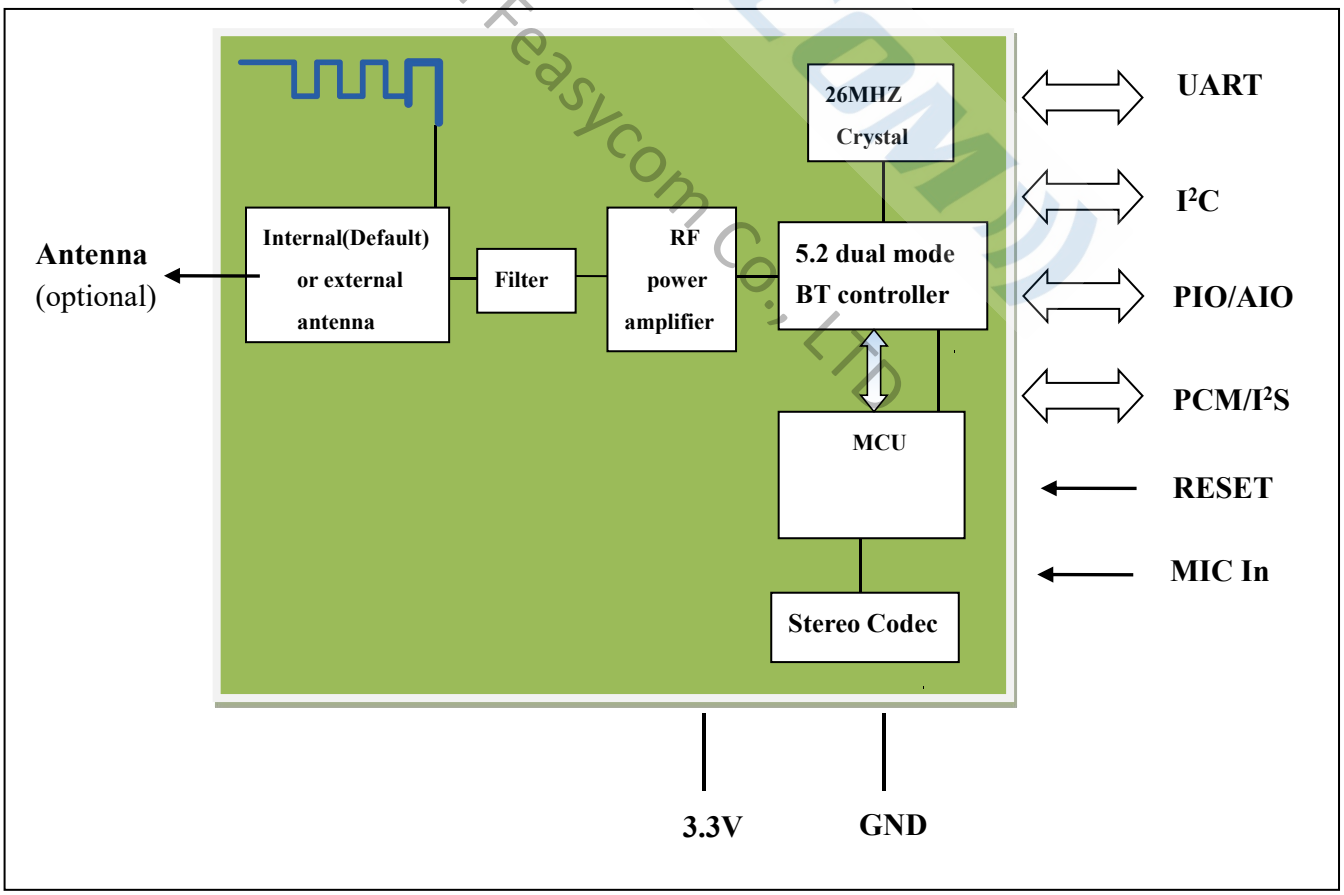


Figure 1

1.2 Feature

- Fully qualified Bluetooth 5.2/4.2/3.0/2.1/2.0/1.2/1.1
- Postage stamp sized form factor,
- Class 1 support (high output power)Low power
- Class 1 support(high output power)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921Kbps,.
- UART, I^2C, PCM/I^2S data connection interfaces.
- Profiles including HS/HF, A2DP, AVRCP, OPP, DUN, SPP, HID,BLE
- RoHS compliant
- FCC, CE Certified

1.3 Application

- Cable replacement
- Portable Multimedia players
- High quality stereo headsets
- High quality mono headsets
- Hands-free car kits
- Wireless speakers
- Bluetooth-Enable Automotive Dashboards
- VOIP handsets
- Medical devices
- Barcode and RFID scanners
- Industrial devices

2. GENERAL SPECIFICATION

General Specification	
ChipSet	CSR8811
Product ID	FSC-BT909C
Dimension	13mm(W) x 26.9mm(L) x 2.2mm(H) (Tolerance: ±0.1mm)
Bluetooth Specification	Bluetooth V5.2 (Dual Mode)
Power Supply	3.3 Volt DC
Output Power	18.5 dBm (Class 1)
Sensitivity	-86dBm@0.1%BER
Frequency Band	2.402GHz -2.480GHz ISM band
Modulation	GFSK, π/4-DQPSK, 8-DPSK
Baseband Crystal OSC	26MHz
RF Input Impedance	50 ohms
Antenna	Integrated chip antenna
Interface	Data: UART (Standard), I²C Audio: MIC In (Standard), PCM/I²S Others: PIO, AIO, Touch sensor, PWM. USB 2.0
Profile	SPP, GATT(BLE Standard) MFI, Airsync, ANCS, iBeacon, HID HS/HF, A2DP, AVRCP
Temperature	-20ºC to +85ºC
Humidity	10%~95% Non-Condensing
Environmental	RoHS Compliant
MSL grade:	MSL 3
ESD grade	Human Body Model: Class-2 Machine Model: Class-B

Table 1

3. PHYSICAL CHARACTERISTIC

- Dimension： 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

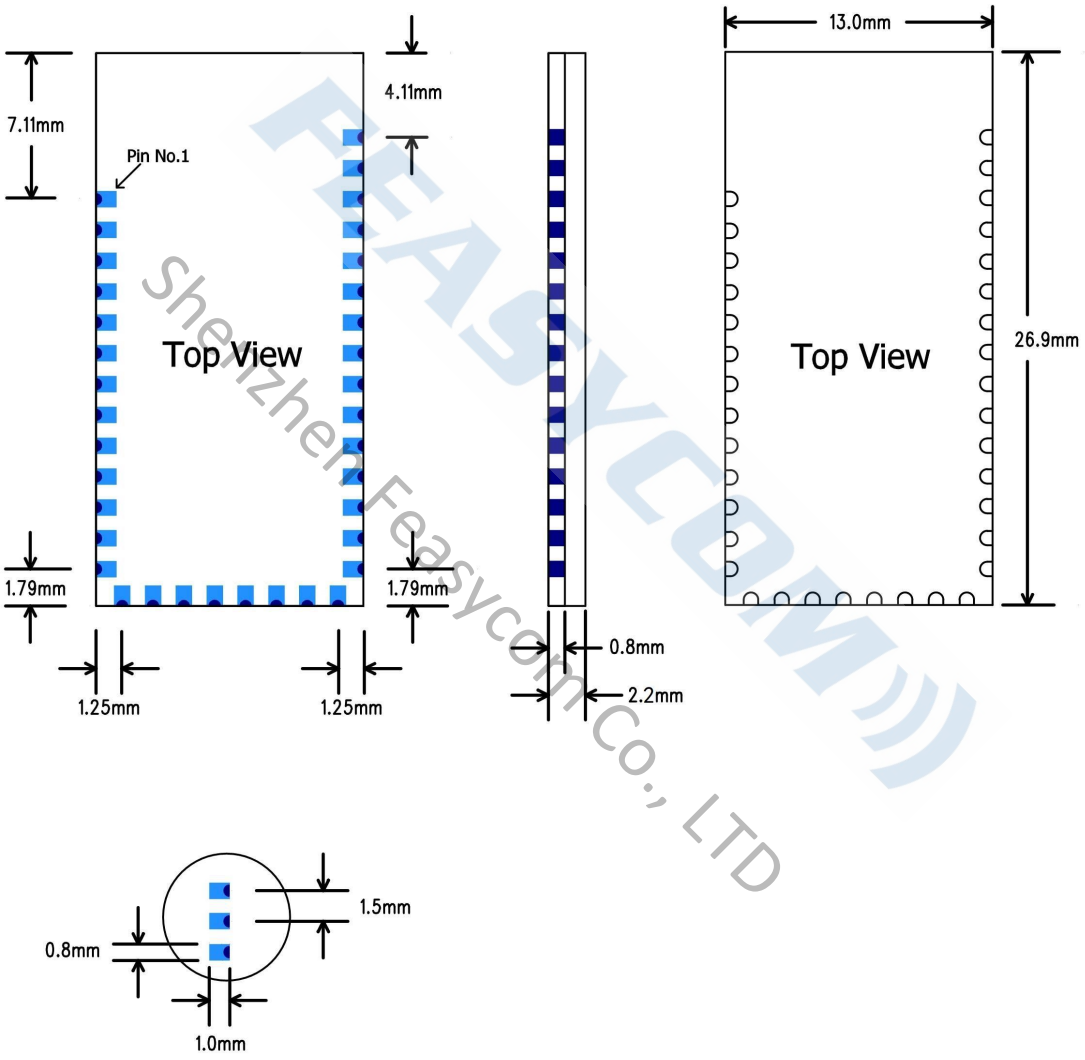


Figure 2

4. PIN DEFINITION DESCRIPTIONS

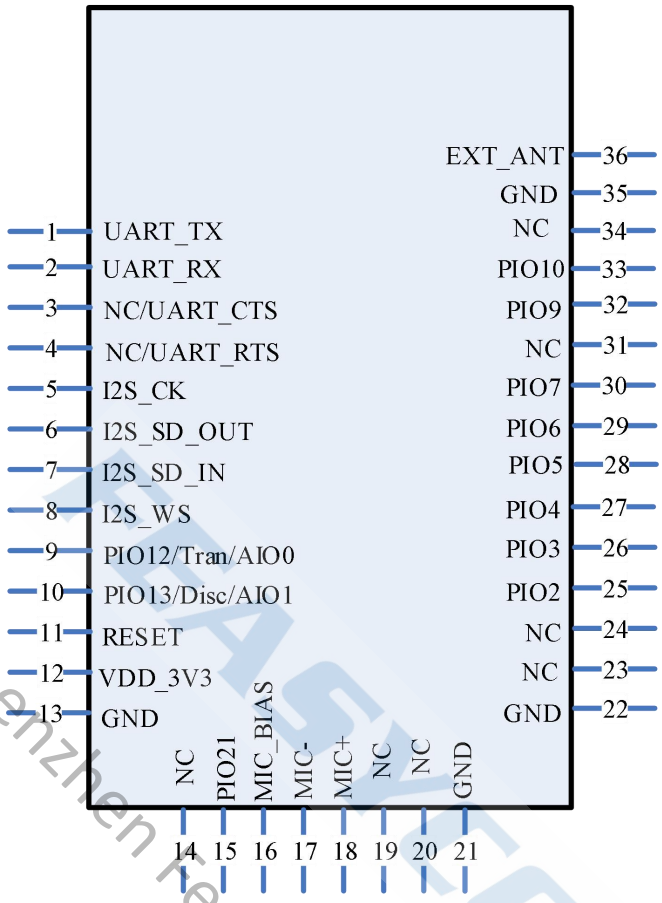


Figure 3: FSC-BT909C PIN Diagram

Pin NO.	Pin Name	Type	Pin Descriptions
1	UART_TX	CMOS output	UART data output
2	UART_RX	CMOS input	UART data input
3	UART_CTS	CMOS input	UART clear to send active low (NC by Default)
4	UART_RTS	CMOS output	UART request to send active low(NC by Default)
5	I2S_CK	Bi-directional	I²S CLK (BCLK)
6	I2S_SD_OUT	Bi-directional	I²S Data Output
7	I2S_SD_IN	Bi-directional	I²S Data Input
8	I2S_WS	Bi-directional	I²S Chip Select For Synchronous Serial Interface
9	PIO12/Tran/AIO0	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU change UART transmission mode.
10	PIO/13Disc/AI	I/O	Programmable input/output line

	O1		Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth.
11	RESET	CMOS input	Reset if low. Input debounced so must be low for >5ms to cause a reset.
12	VDD_3V3	VDD	Power supply voltage 3.3V
13	GND	VSS	Power Ground
14	NC	--	--
15	PIO21	Bi-directional	Programmable input/output line
16	MIC_BIAS	VDD	MIC_VDD
17	MIC-	Analogue Input	MIC- Input
18	MIC+	Analogue Input	MIC+ Input
19	NC	--	NC—Do not to GND
20	NC	--	NC—Do not to GND
21	GND	VSS	Power Ground
22	GND	VSS	Power Ground
23	NC	--	--
24	NC	--	--
25	PIO2	Bi-directional	Programmable input/output line
26	PIO3	Bi-directional	Programmable input/output line
27	PIO4	Bi-directional	Programmable input/output line **Alternative Function: PA_EN pin, active high**
28	PIO5	Bi-directional	Programmable input/output line
29	PIO6	Bi-directional	Programmable input/output line Alternative Function: I^2C Serial Clock input/output
30	PIO7	Bi-directional	Programmable input/output line Alternative Function:I^2C Serial Data input/output
31	NC	--	--
32	PIO9	Bi-directional	Programmable input/output line Alternative Function: LED(Default)
33	PIO10	Bi-directional	Programmable input/output line Alternative Function: BT Status(Default)
34	NC	--	--
35	GND	VSS	Power Ground

36	EXT_ANT	RF signal output	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

Table 2

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

The module should not continuously run under extreme conditions. The absolute maximum ratings are summarized in Table below. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Temperature/Voltage	Min	Max	Unit
Storage temperature	-40	85	°C
Operating temperature	-20	85	°C
Supply voltage	-0.3	3.6	V
Terminal voltages	VSS - 0.4	Vdd + 0.4	V

Table 3

5.2 Absolute Recommended Operating Conditions

The recommended operating conditions are summarized in Table below.

Temperature/Voltage	Min	Typ	Max	Unit
Operating temperature	-20	25	85	°C
Supply voltage	--	3.3	--	V
Terminal voltages	0		Vdd	V

Table 4

5.3 Terminal Characteristics

FSC-BT909C's terminal characteristics are summarized Table below.

Characteristics	Min	Typ	Max	Unit
I/O static characteristics				
VIL input logic level low	-	-	0.3V_{DD}	V
VIH input logic level high	0.4V_{DD}	-	-	V
V_{HYS} input hysteresis	-	10% V_{DD}	-	V

I_{lkg} input leakage current	-	-	±1	uA
R_{PU} Weak pull-up equivalent resistor	30	40	50	KΩ
R_{PD} Weak pull-down equivalent resistor	30	40	50	KΩ
C_{IO} pin capacitance	-	5	-	pF
VOL output logic level low	-	-	0,2	V
VOH output logic level high	Vdd -0.4	-	-	V
NRST pin characteristics				
VTH,res threshold voltage	1.65	1.8	VDD	V
RIRES input resistance	-	10	-	kΩ
CIRES input capacitance	-	100	-	nF

Table 5

5.4 Current Consumption

FSC-BT909C's current consumption is summarized in Table below.

Operation Mode	Connection Type	Average	Unit
Discoverable	Inquiry/page:640mS interval ,11.25mS window Advertising :152.5mS interval	28	mA
ACL	Active Mode	34	mA
	File transfer ,throughput	44	mA
SCO	Active Mode	36	mA
LE Connected	20mS Interval	30	uA
	File transfer ,throughput	36	mA
ACL & LE Both connected	ACL:1280mS interval LE:240mS interval	1.7	mA
Maximum Current	Send 2441MHZ fixed frequency signals	~225	mA

Table 6

5.5 Radio Characteristics

5.5.1 Transmitter Radio Characteristics

TX output is guaranteed to be unconditionally stable over the guaranteed temperature range. Refer to Table below. Measurement conditions: T = 20℃, Vdd = 3.3V.

Item	Typical Value	Bluetooth Specification	Unit

Maximum output power1,2	+18.5	-6 to 20	dBm
RF power control range	34	≧16	dB
20dB bandwidth for modulated carrier	788	≦1000	kHz
Adjacent channel transmit power F = F0 ± 2MHz	-36	≦ 20	dBm
Adjacent channel transmit power F = F0 ± 3MHz	-45	-40	dBm
Adjacent channel transmit power F = F0 ± > 3MHz	-51	-40	dBm
Δf1avg Maximum Modulation	163	140<f1avg<175	kHz
Δf2max Maximum Modulation	158	115	kHz
Δf1avg / Δf2avg	0.91	≧0.80	-
Initial carrier frequency tolerance	13	≦75	kHz
Drift Rate	8	≦20	kHz/50μs
Drift (single slot packet)	7	≦ 25	kHz
Drift (five slot packet)	9	≦ 40	kHz
2nd Harmonic content	-65	≦ -30	dBm
3rd Harmonic content	-45	≦ -30	dBm

Table 7

5.5.2 Receiver Radio Characteristics

RX input is guaranteed to be unconditionally stable over the guaranteed temperature range. Refer to Table below. Measurement conditions: T = 20℃, Vdd = 3.3V.

	Frequency(GHz)	Typ.	Unit	Bluetooth Specification
Sensitivity@0.1% BER for all packet types	2.402	-87	dBm	<-75dBm
	2.441	-88	dBm	
	2.480	-86	dBm	
BER@ Maximum received signal(-20dBm)	2.402	0	dBm	<0.1%
	2.441	0	dBm	
	2.480	0	dBm	

Table 8

6. Interface Characteristics

6.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT909C is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

Signal name	Driving source	Description
UART-TX	FSC-BT909C module	Data from FSC-BT909C module
UART-RX	Host	Data from Host
UART-RTS	FSC-BT909C module	Request to send output of FSC-BT909C module
UART-CTS	Host	Clear to send input of FSC-BT909C module

Table 9

Possible UART Settings

Property	Possible Values
Baud Rate	1200bps to 921Kbps
Flow Control	RTS/CTS or None
Data bit length	8bits
Parity	None, Odd or Even
Number of Stop Bits	1 or 2

Table 10

Default Data Format

Property	Possible Values
Baud Rate	115.2Kbps
Flow Control	None
Data bit length	8bit
Parity	None
Number of Stop Bits	1

Table 11

6.2 PCM/I²S Interface

The I²S can be operated in master or slave mode, in full duplex and simplex communication modes and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I²S can be served by the DMA controller.

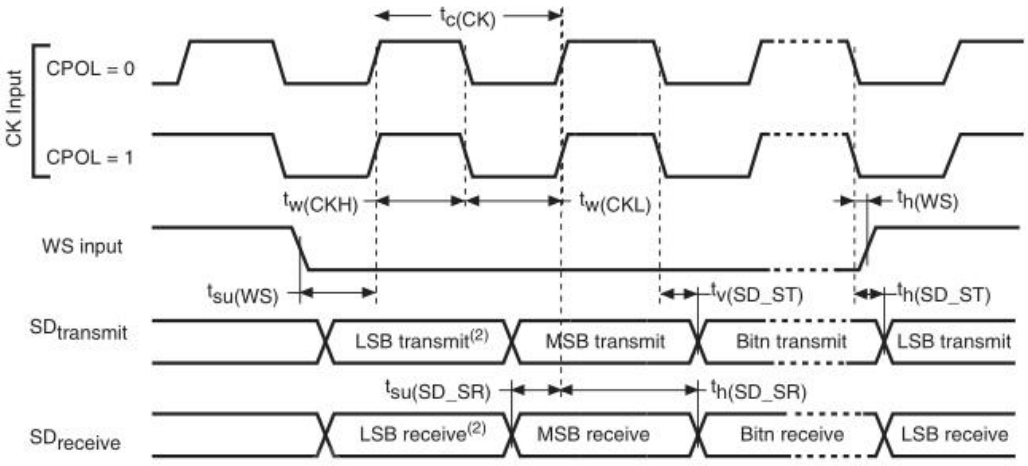
6.3 I²S dynamic characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	6	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	7.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	27	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization.
2. The maximum value of 256xFs is 42 MHz (APB1 maximum frequency).

Table 12 I²S dynamic characteristics

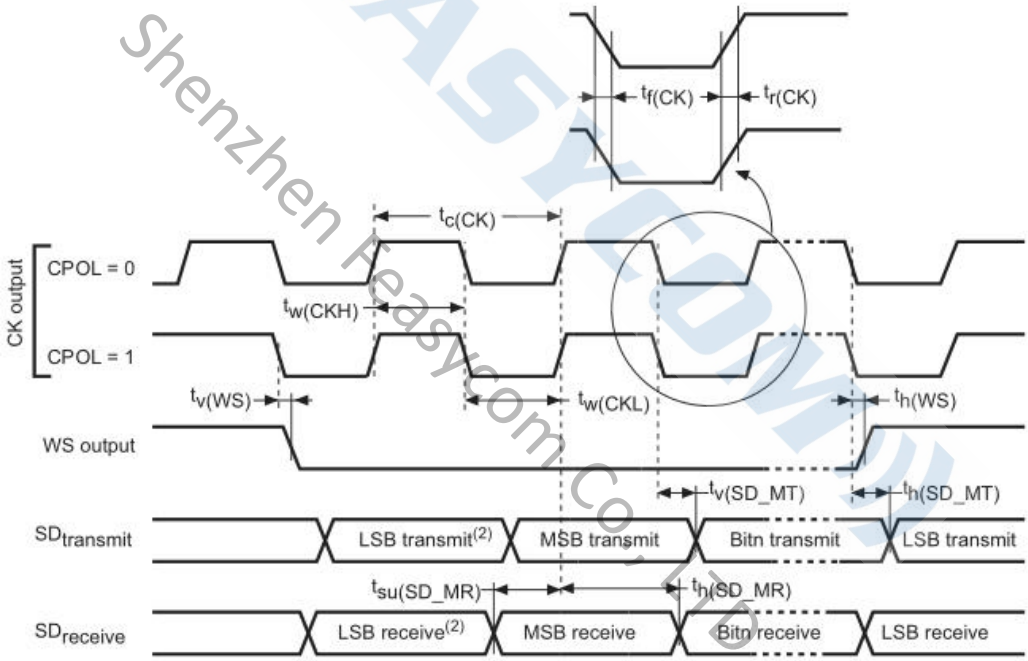
Note: Refer to the I2S section of the reference manual for more details on the sampling frequency(F_S).
f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.



360

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 4: I²S slave timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 5: I²S master timing diagram (Philips protocol)

6.4 AIO , PIO lines and I²C

Up to 16 programmable bidirectional input/output (I/O) can be used.

Two general purpose analogue interface pin can be used.

PIO6 and PIO7 can be used as I2C interface.

Inter-Integrated Circuit Interface (I²C)

I²C bus interfaces can operate in multi-master and slave modes. They can support the standard (up to 100 kHz) and fast (up to 400 kHz) modes. The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative. They also support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SMBus 2.0/PMBus.
The devices also include programmable analog and digital noise filters

Analog to Digital Converter (ADC)
One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.
The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.
To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1,TIM2, TIM3, TIM4 or TIM5 timer.

6.5 Audio Interface

FSC - BT909C built-in a low power, high quality stereo codec.
The Codec main features as follows:

- DAC with auto attenuate : 124dB SNR; without auto mute: 113dB SNR, (A-weighted) @ 0dB gain, 1.8V and -89dB THD @ 20mW and R L = 32Ω, DAC playback to headphone output mode.
- ADC : 101dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48kHz and -91dB THD , 1.8V, MIC gain 0dB, OSR 128x.
- Dynamic Range Compressor (DRC).
- Programmable Biquad filter.
- 1 Differential Analog Mic input, Line-input, or two single-ended Mic input.
- Class G Headphone Amplifier(28mW @ 32Ω,1% THD+N).

6.6 Audio Electrical Characteristics

Conditions: $V_{DD}A = V_{DD}C = 1.8V$; $V_{DD}B = V_{DD}MIC = 3.3V$.
R_L(Headphone)=32Ω, f=1kHz, MCLK=12.88MHz, unless otherwise specified.
Limits apply for T_A= 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
ISD	Shutdown Current	V_{DD}A in Shutdown Mode	0.2	1	µA
		V_{DD}A When V_{DD}C=1.2V	17.2		
		V_{DD}B	0.2	1	
		V_{DD}C	2	10	
		V_{DD}MIC	0.2	1	
I_{DD}	Standby Mode	MCLK off, Jack Insertion, IRQ enabled	5		µA
		Headphone Amplifier			
P_O	Output Power	Stereo R_L = 32Ω, DAC Input, CPV_{DD}= 1.8V, f=1kHz, 22kHz BW, THD+N = 1%(CSP package), w. headset switch	TBD		mW
		Stereo R_L = 32Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (QFN package), w. headset switch	28		mW
		Stereo R_L = 16Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (CSP Package), w. headset switch	TBD		mW
		Stereo R_L = 16Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (QFN Package), w. headset switch	35		mW
THD+N	Total Harmonic Distortion + Noise	R_L = 32Ω, f=1kHz, P_O = 20mW, w. headset switch	-89		dB
SNR	Signal to Noise Ratio	VOUT = 1VRMS, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1kHz, A-Weighted), w. headset switch	113		dB
		VOUT = 1 V_{RMS}, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1kHz, A-Weighted, auto mute enabled, w. headset switch	124		dB
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} Input Referred, HP_GAIN = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to V_{DD}A	81		dB
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, -1dBFS, Gain = 0dB, f= 1kHz, MIC/GND Switching Off without HCS	88		dB
		Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1kHz, MIC/GND Switching On with HCS (QFN)	91		dB

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
		Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1kHz, MIC/GND Switching On with HCS (CSP)	TBD		dB
	Interchannel Level Mismatch	Head phone Right and Left Channel Difference with 0dBFS Input Sweap from 20Hz to 20KHz	+/- 0.1		dB
	Frequency Response	F = 20Hz ~ 20KHz	+/-0.005		dB
e_{OS}	Output Noise	DAC_Gain = 0dB, HP_Gain = 0dB, f_S=48kHz, OSR_{DAC} = 128, A-Weighted	2.2		uV_{RMS}
	Out of Band Noise Level	BW=400Hz to 500KHz	-86		dB
V_{OS}	Output Offset Voltage	HP_Gain = 0dB, DAC_Gain= 0dB, DAC Input	0.1	±0.5	mV
	Power Consunption	No Load, No Signal, Amp on f_S = 48kHz, Stereo DAC On, Amp On, P_{OUT} = 0mW. R_L = 32Ω	5.7		mW
	Pop and Click Noise	Into or out of DAC to Headphone shutdown, Headphone Impedance &Crosstalk detection disabled	.1		mVrms
	Ground Switch ON resistance	ON resistance between JKR2 and GND or JKSLV and GND(QFN)	.09		ohm
		ON resistance between JKR2 and GND or JKSLV and GND(CSP)	TBD		ohm
	Loading Capacitance	External capacitance at HPL and HPR		<500	pF
		ADC			
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1KHz, fs = 48KHz, Mono Differential Input	-91		dB
		MIC Input, MIC_GAIN = 30dB, Volume = 0dB, Vin=28.5Vrms, f=1k, Digital Gain = 0dB, Mono Differential Input	-80		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 8KHz, Mono Differential Input	101		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 8KHz, Mono Differential Input	98		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP} applied to V_{DD}A, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	78		dB
CMRR	Common Mode Rejection Ratio	Differential Input 100Vrms, PGA gain = 20dB, frequency sweep from 20Hz to 20KHz	64		dB
FS_{ADC}	ADC Full Scale Input Level	V_{DD}A= 1.8V	1		V_{RMS}
	Minimum Input Impedance		12		KOhm
	Frequency Response	f = 20Hz ~ 20KHz	+/-0.02		dB
	Power Consumption	No Load, No Signal, ADC on, PGA on, fS = 44.1kHz	5.4		mW

Table 13: Analogue Inputs to ADC out & Analogue Outputs

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

The re-flow profiles are illustrated in Figure 4 and Figure 5 below.

- Follow: IPC/JEDEC J-STD-020 C
- Condition:
  - Average ramp-up rate(217℃ to peak):1~2℃/sec max.
  - Preheat:150~200C,60~180 seconds
  - Temperature maintained above 217℃:60~150 seconds
  - Time within 5℃ of actual peak temperature:20~40 sec.
  - Peak temperature:250+0/-5℃ or 260+0/-5℃
  - Ramp-down rate:3℃/sec.max.
  - Time 25℃ to peak temperature:8 minutes max
  - Cycle interval：5 mintutes

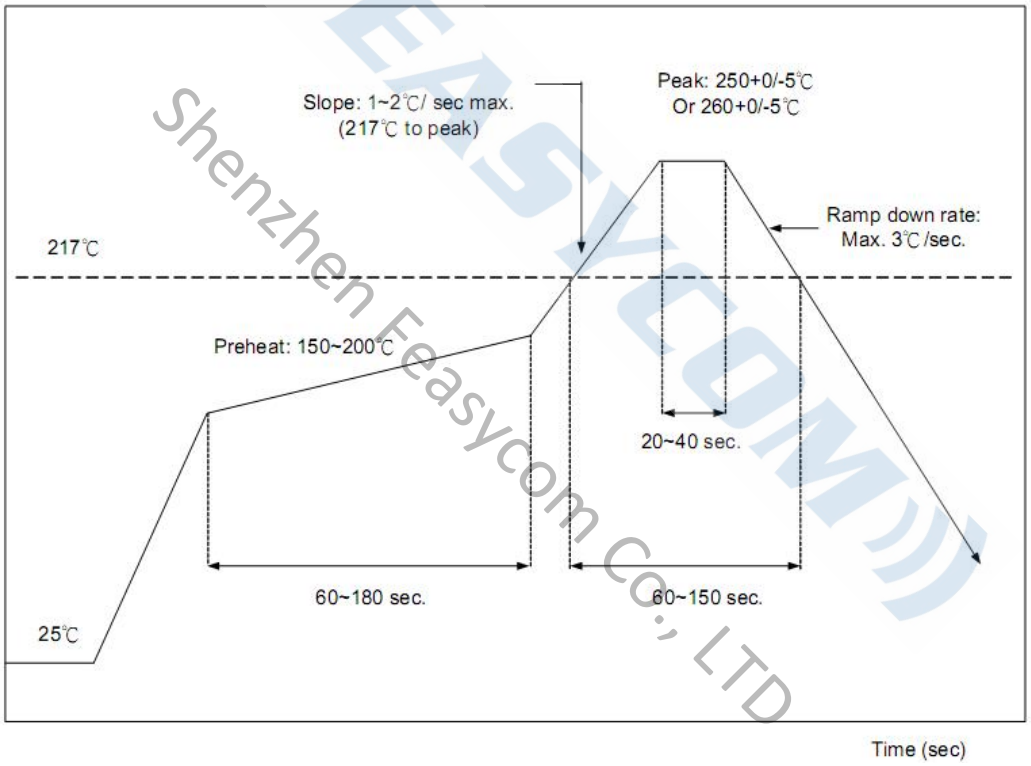


Figure 6: Typical Lead-free Re-flow Solder Profile

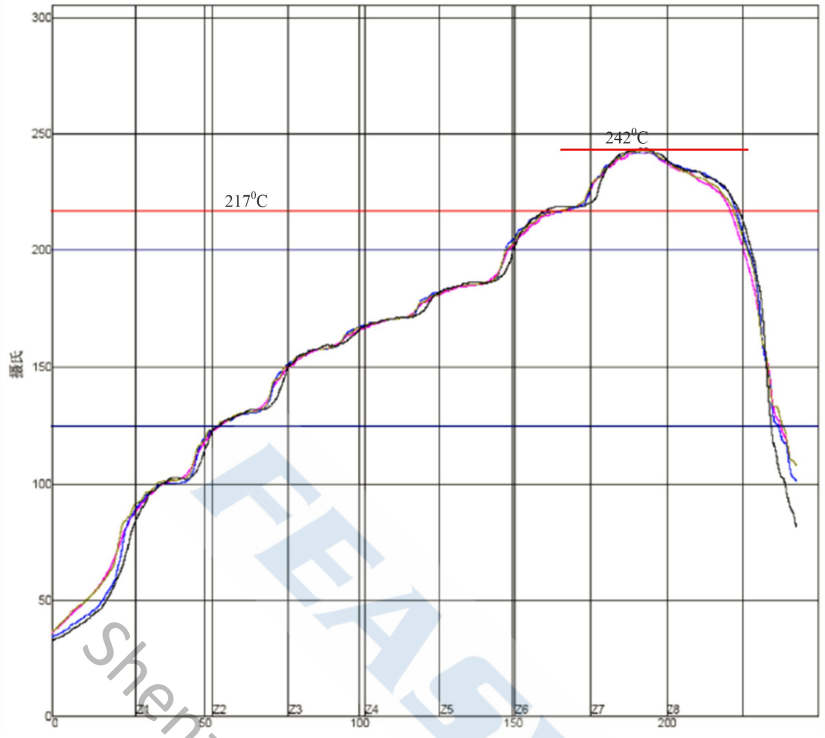


Figure 7: Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow.

FSC-BT909C will withstand up to two re-flows to a maximum temperature of 245°C.

8. Reliability and Environmental Specification

8.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －30℃ space for 1 hour and then move to +85℃ space within 1minute, after 1 hour move back to －30℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

8.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

8.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

8.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

8.5 Packaging information

After unpacking, the module should be stored in environment as follows:

Temperature: 25℃ ± 2℃

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

9. Layout and Soldering Considerations

9.1 Soldering Recommendations

FSC-BT909C is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

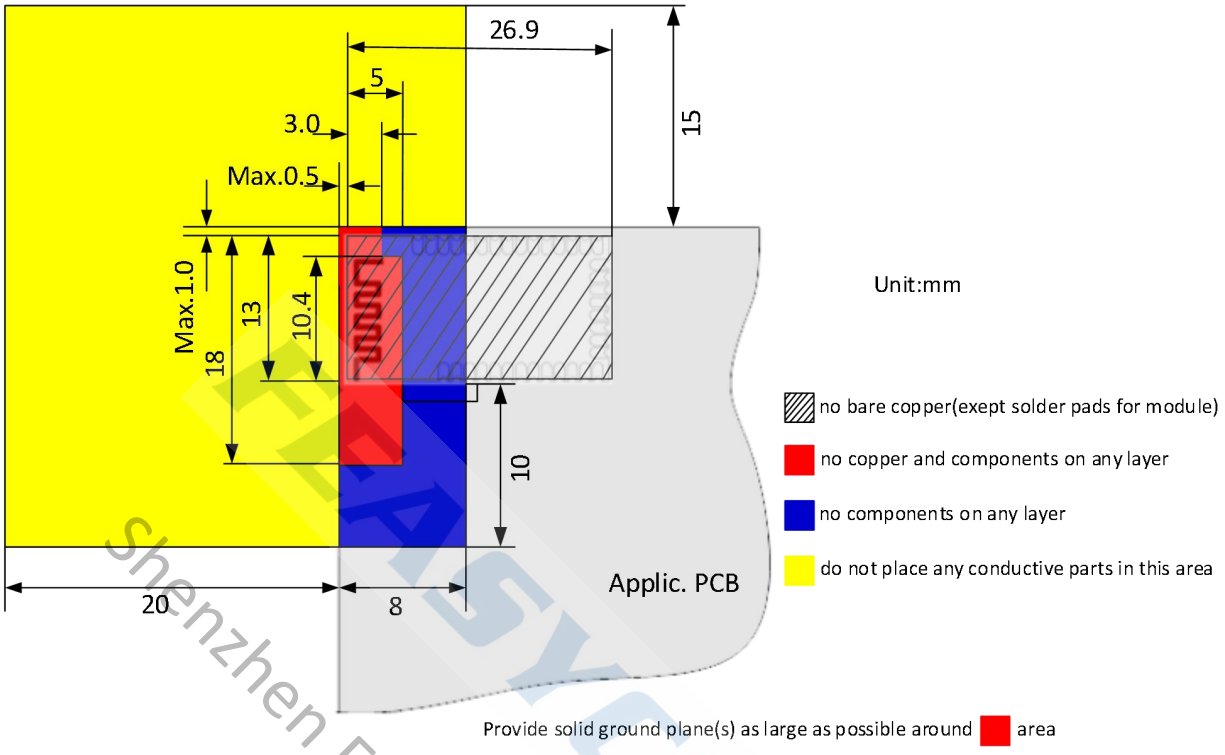


Figure 8: FSC-BT909C Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

10. Product Packaging Information

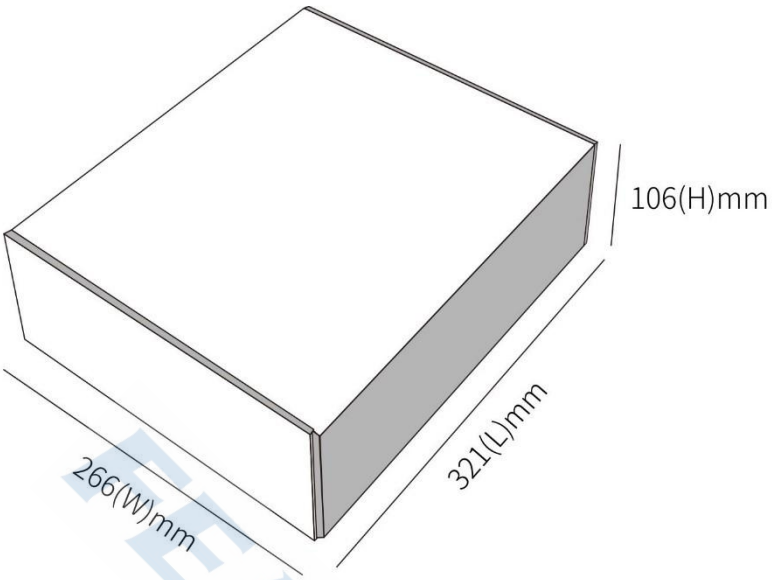
10.1 Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 9: Product Packaging Information (Tray)

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

Figure 10: Packing Box

11. Application Schematic